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IN THE CLAIMS

**Claim 1 (currently amended)** A method of fabricating an FET device comprising the steps of:  
    forming a semiconductor structure comprising a source region, a drain region over a horizontal surface of a substrate comprising an insulating material;  
    forming a channel structure over the horizontal surface of the substrate connecting between the drain region and the source region, with the channel structure comprising a horizontal horizontally oriented, planar semiconductor channel fin composed of a semiconductor material, with the planar fin being formed above a vertical fin, with the vertical fin being composed of a material selected from the group consisting of a semiconductor material and an insulating material, with the planar fin and the vertical fin having a T-shaped cross-section, the vertical fin having a proximal edge and a distal edge, with the proximal edge in contact with the horizontal surface of the substrate and with the planar fin in contact with the distal edge of the vertical fin;  
    forming a gate dielectric layer over exposed surfaces of the channel structure; and  
    forming a gate electrode straddling the channel gate dielectric and the channel structure.

**Claim 2 (currently amended)** The method of claim 1 wherein the channel structure comprises a vertical fin and a planar fin both is composed of a semiconductor material selected from the group consisting of Ge and SiGe.

**Claim 3 (currently amended)** The method of claim 1 wherein the channel structure comprises a vertical fin is composed of an insulating material selected from the group consisting of silicon oxide and silicon nitride, and a planar fin composed of a semiconductor material.

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**Claim 4 (currently amended) The method of claim 1 including the steps as follows:**

**forming a sacrificial layer over the horizontal surface of the substrate prior to forming the channel structure;**

**forming a patterned window extending through the sacrificial layer down to the horizontal surface of the substrate for shaping the vertical fin of the channel structure;**

**depositing a semiconductor layer filling the patterned window to form the vertical fin of the channel structure and forming a blanket semiconductor layer covering the sacrificial layer;**

**forming a channel mask over the blanket semiconductor layer aligned with the vertical fin of the channel structure;**

**etching away portions of the blanket semiconductor layer aside from the channel mask to form the planar fin;**

**whereby the channel structure comprises [[a]] the vertical fin and [[a]] the planar fin.**

**Claim 5 (currently amended) The method of claim 4 wherein the vertical fin and [[a]] the planar fin are both composed of silicon.**

**Claim 6 (currently amended) The method of claim 4 wherein the vertical fin and [[a]] the planar fin are both composed of a material selected from the group consisting of Ge and SiGe.**

**Claim 7 (previously presented) The method of claim 4 wherein:**

**the semiconductor material comprises silicon (Si); and**

**the sacrificial layer comprises silicon-germanium (SiGe).**

**Claim 8 (currently amended) The method of claim 4 wherein:**

**the semiconductor material comprises a material selected from Ge and SiGe; and**

**the sacrificial layer comprises a material selected from the group consisting of silicon (Si) and SiC.**

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**Claim 9 (currently amended) The method of claim 1 including the steps as follows:**

forming a sacrificial layer over the horizontal surface of the substrate prior to forming the channel structure;

forming a patterned window extending through the sacrificial layer down to the horizontal surface of the substrate for shaping the vertical fin of the channel structure;

depositing a dielectric layer filling the patterned window to form the vertical fin of the channel structure and forming a blanket semiconductor layer covering the sacrificial layer;

forming a channel mask over the blanket semiconductor layer aligned with the vertical fin of the channel structure;

etching away portions of the blanket semiconductor layer aside from the channel mask to form the planar fin;

whereby the channel structure comprises [[a]] the vertical dielectric fin and [[a]] the planar semiconductor fin.

**Claim 10 (currently amended) The method of claim 9 wherein the planar fin is composed of a material selected from the group consisting of silicon (Si), germanium (Ge) and SiGe.**

**Claim 11 (previously presented) The method of claim 9 wherein the planar fin is composed of silicon (Si) and the sacrificial layer is composed of SiGe.**

**Claim 12 (currently amended) The method of claim 9 wherein the planar fin is composed of SiGe and the sacrificial layer is composed of ~~comprises~~ a material selected from the group consisting of silicon (Si) and SiC.**

**Claim 13 (currently amended) The method of claim 9 wherein the vertical fin is composed of a material selected from the group consisting of silicon dioxide and silicon nitride.**

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**Claim 14 (currently amended) An FET device comprising:**

a semiconductor structure comprising a source region, a drain region over a horizontal surface of a substrate comprising an insulating material;

a channel structure over the horizontal surface of the substrate connecting between the drain region and the source region, with the channel structure comprising a horizontal horizontally oriented, planar semiconductor channel fin composed of a semiconductor material, with the planar semiconductor channel fin being positioned above a vertical fin, with the vertical fin being composed of a material selected from the group consisting of a semiconductor material and an insulating material, with the planar fin and the vertical fin having a T-shaped cross-section, the vertical fin having a proximal edge and a distal edge, with the proximal edge in contact with the horizontal surface of the substrate and with the planar fin in contact with the distal edge of the vertical fin;

a gate dielectric layer over exposed surfaces of the channel structure; and

a gate electrode straddling the channel gate dielectric and the channel structure.

**Claim 15 (currently amended) The FET device of claim 14 wherein the channel structure comprises [[a]] the vertical fin and [[a]] the planar fin both composed of a semiconductor material.****Claim 16 (currently amended) The FET device of claim 14 wherein the channel structure comprises [[a]] the vertical fin composed of an insulating material selected from the group consisting of silicon oxide and silicon nitride and [[a]] the planar fin composed of a semiconductor material selected from the group consisting of silicon (Si), germanium (Ge) and SiGe.****Claim 17 (currently amended) The FET device of claim 14 wherein the vertical fin and [[a]] the planar fin are both composed of silicon.**

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**Claim 18 (currently amended) The FET device of claim 14 wherein the vertical fin and [[a]] the planar fin are both composed of a material selected from Ge and SiGe.**

**Claim 19 (currently amended) The FET device of claim 14 wherein the vertical fin is composed of a dielectric and the planar fin is composed of a material selected from the group consisting of silicon (Si), germanium (Ge) and SiGe.**

**Claim 20 (currently amended) The FET device of claim 14 wherein the vertical fin is composed of a dielectric and the planar fin is composed of silicon (Si), ~~and the sacrificial layer is composed of SiGe.~~**